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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/616,021 | 07/09/2003 | Jri Lee | G&C 30448.116-US-U1 | 1118 |

22462 7590 12/13/2005

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| EXAMINER | |
|---|---|
| WONG, LINDA | |
| **ART UNIT** | **PAPER NUMBER** |
| 2634 | |

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/616,021 | LEE ET AL. | |
| | Examiner | Art Unit | |
| | Linda Wong | 2634 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

### *Claim Rejections - 35 USC § 102*

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1,2,6,8-12,16,18-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Song et al (Publication: "4-G/bs Clock and Data Recovery Using Four-Phase 1/8-Rate Clock").

   a. **Claim 1**, Song et al discloses phase locked loop (PLL) comprising a multi-phase voltage controlled oscillator (Fig. 1, label VCO) for accepting a control signal (Fig. 1, output from label LPF) and changing a frequency of a clock signal output from the VCO (Fig. 1, labels CK0-CK3) in response thereto, wherein the voltage-controlled oscillator outputs a plurality of phases of the clock signal (Fig. 1, labels CK0-CK3), a phase detector (Fig. 1, label Four-Phase Detector) for sampling an input data signal (Fig. 1, label NRZ data) using the clock signal received from the VCO (Fig. 1, labels CK0-CK3) and generating a plurality of output signals (Fig. 1, labels D0-D3) in response to the input data signal having a different frequency compared to the plurality of clock signals (Fig. 1, labels

CK0-CK3 and NRZ data) and the input data is retimed (page 240, right column, lines 6-8) and demultiplexed (Fig. 1, label Four-Phase Detector Performing 1:4 DEMUX) into the output signal (Fig. 1, labels D0-D3), a Voltage to current converter (Fig. 1, label Charge pump) and a loop filter (Fig. 1, label LPF). The phase detector detects an edge or transition in the input data signals and whether they are late or early. (page 240, right column and page 241, left column).

b. **Claim 2** inherits the limitations of claim 1.

c. **Claim 6**, Song et al discloses using leading and trailing edges of the phases of the clock signal to sample the input data signal (pages 240 and 241, Sub-Heading: Four Phase Detector)

d. **Claim 8**, Song et al discloses a VCO with a ring oscillation structure, which inherently has a travel time of a wave around a loop. (Fig. 2a)

e. **Claim 9**, Song et al discloses inductor elements of the VCO grouped into a differential structure (Fig. 2b and c) and –Gm cells are placed close to the nodes of the VCO (Fig. 2b and c)

f. **Claim 10**, Song et al discloses a VCO comprising a switch connected to each port. Although Song et al discloses a current source structure for the switch, it is well known that at current source structure can be built using transistors or differential pairs. To place inductors as resistive elements to the load of the differential pair or transistors built to be equivalent to the current source, it

would be obvious to one skilled in the art, based on designers choice, to use inductors as opposed other resistive elements.

g. **Claim 11** inherits all the limitations of claim 1.

h. **Claim 12** inherits all the limitations of claim 2.

i. **Claim 16** inherits all the limitations of claim 6.

j. **Claim 18** inherits all the limitations of claim 8.

k. **Claim 19** inherits all the limitations of claim 9.

l. **Claim 20** inherits all the limitations of claim 10.

3. **Claims 3-4,7, 13-14 and 17** are rejected under 35 U.S.C. 102(e) as being anticipated by Song et al (Publication: "4-G/bs Clock and Data Recovery Using Four-Phase 1/8-Rate Clock") in view of Savoj et al (Publication: "A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection").

a. **Claim 3**, Savoj et al discloses phase detector using a half-quadrature phases of the clock signal provided by the VCO to sample the input data signal for determining asynchronous transitions between the input data signal and the clock signals. (page 3, left column, lines 13-14, 26-32, 50-59 and right column, lines 1-9) It would be obvious to one skilled in the art to incorporate the half-quadrature phases of the clock signals as disclosed by Savoj et al to Song et al to reduce cost and reduce jitter.

b. **Claim 4**, Song et al discloses a plurality of flip-flops to strobe the data input based on a plurality of phases of the clock signals. (Fig. 3)

c. **Claim 7**, Savoj et al discloses a VCO sustains a phase separation of 180 degrees at diagonally-opposite nodes, providing 45 degrees phase steps in between the clock signals. (Fig. 5.3.1, label 0,45,90,135 degrees and Fig. 5.3.2(a))

d. **Claim 13** inherits all the limitations of claim 3.

e. **Claim 14** inherits all the limitations of claim 4.

f. **Claim 17** inherits all the limitations of claim 7.

4. **Claims 5 and 15** are rejected under 35 U.S.C. 102(e) as being anticipated by Song et al (Publication: "4-G/bs Clock and Data Recovery Using Four-Phase 1/8-Rate Clock") in view of Nakamura et al (Publication: "A 6Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock").

a. **Claim 5**, Although Song et al does not disclose a phase detector as recited in claim 5, Nakamura discloses a PLL comprising a phase detector comparing every two adjacent or consecutive samples stored in the two adjacent flip-flops by using an XOR gate (Fig. 1 and Fig. 3), which generates a net output current if the two adjacent samples are unequal, thereby indicating that an edge or transmission has occurred in the input signal. (page 196, Sub-heading: Phase Detecting 1:2 Demux Module)

b. **Claim 15** inherits all the limitations of claim 5.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. "50-Gb/s SiGe BiCMOS 4:10 Multiplexer and 1:4 Demultiplexer for Serial Communication Systems" Meghelli, Mounir, Rylyakov, Alexander V. and Shan, Lei, IEEE Journal of Solid-State Circuits, Vol. 37, No. 12, December 2002

   b. "Integrated Circuits for 80 Gbit/s Data Transmission", http://www.iaf.fraunhofer.de/pdf/jahresbericht-2002/integrated.pdf

   c. Duffy et al (US Patent No.: 6560306)

   d. "4-bit Multiplexer/Demultiplexer Chip Set for 40-Gbit/s Optical Communications Systems", Ishii et al. IEEE Radio Frequency Integrated Circuits Symposium, 2003 IEEE.

   e. "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz ft Silcon Bipolar Technology", Wurzer et al, IEEE Journal of Solid-State Circuits, Vol. 34, No. 9, September 1999

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong

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